REMARKS

In the Office Action, Claims 8, 9, 12-15, 17, 19-21 and 30-32 are pending in the present application, were examined, and stand rejected. In this response, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 8, 9, 12-15, 17, 19-21 and 30-32 in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Examiner has rejected Claims 8-9, 12-14 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,477,623 ("Jeddeloh") in view of U.S. Patent No. 6,625,673 issued to Dickey ("Dickey").

Regarding Claim 8, Claim 8 is amended to ~~recites~~ recite the following claim ~~feature~~features, which ~~is~~ are neither taught nor suggested by the combination of Jeddeloh in view of Dickey:

> populating entries within a conversion table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses to enable access to the main memory above a physical address range limit imposed by a register/bus width. (Emphasis added.)

using the conversion table to translate a virtual address from the graphics controller to a first physical address for access to the main memory; and

using the conversion table to translate a virtual address from the bus controller to a second physical address for access to the main memory;

> wherein the second physical address has a greater number of bits than the virtual address from the graphics controller and the second physical address has a greater number of bits than the virtual address from a bus controller.

As correctly noted by the Examiner, Jeddeloh does not disclose the ~~second~~ first physical address having a greater number of bits than the ~~first~~ virtual address from the graphics controller and the ~~fourth~~ second address having a greater number of bits than the ~~third~~ virtual address from a bus controller, as recited by Claim 8. As a result, the Examiner cites Dickey.

Regarding Dickey, Dickey is devoid of any teachings or suggestions with regards to providing physical address translation and paging to off-chip components, such as, for example, graphics controllers and I/O devices for access to memory above the 4 GB limit imposed by 32-bit bus and register widths. According to the Examiner, Jeddeloh does not explicitly suggest expanding the address space for I/O devices. (*See* page 3 of the Office Action mailed 01/17/2007.) According to the Examiner:

Dickey teaches mapping a first address to a second address, wherein the second address has a greater number of bits than the first address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). (*See* page 3 of the Office Action mailed 01/17/2007.)

Based on the cited passage above, Applicants respectfully submit that the Examiner has incorrectly equated I/O address mapping techniques, as taught by Dickey, with the translation of virtual addresses received from graphics controllers and I/O devices into a translated physical address for access to memory based on, for example, a previously assigned portion of memory using a memory allocation command (e.g., malloc). In other words, as known to those skilled in the art, memory mapped I/O, as taught by Dickey, provides an address assignment mechanism for the various bridges and I/O devices in a computer system. This technique assigns a portion of the processor address space to the various I/O device to enable access to such I/O devices.

For example, to access an I/O device, the processor issues a transaction to a memory address which is detected by, for example, a memory controller or other like device, as mapped to an I/O device. In response to such detection, the memory controller (or in the case of Dickey, the host bridge) identifies that the memory address is mapped to a respective I/O device and directs the transaction to the respective I/O device.

Accordingly, Dickey teaches that:

> Host I/O bridge m . . . translates the (n+l)-bit processor view I/O address to a 32-bit I/O device view I/O address. (Col. 5, lines 1-5).

Hence, the I/O address mapping technique taught by Dickey:

> Provides a pre-assigned address region, which is guaranteed to be available, to each of the I/O device in the system, and thus provide the convenience on-line replacement of various I/O devices having different memory capacity requirements without causing an out-of-address-space problem associated with fragmentation of I/O memory space in the system memory. (Col. 6, lines 17-23)

Therefore, as illustrated ~~in~~ with reference to FIG. 4 of Dickey, the teachings of Dickey are expressly limited to the translation of a processor view address 401 which may be 40 bits into an I/O device view address 403 which is comprised of 32 bits. As described by Dickey:

> The I/O mapping utilizes a greater number of address bits than the address bits available from I/O devices to assign a much larger address space to each device by translating the larger number of bits address from the system to the smaller number of bits address of the I/O devices. (Col. 3, lines 61-66)

However, Applicants respectfully submit that such I/O devices are still limited to access within the 4 GB range as provided by 32-bit addresses. Hence, although Dickey expands the I/O address space for the various bridges and peripheral devices connected to a computer system as taught by Dickey, this expansion is simply limited to the processor's view. In other words, Dickey teaches expansion of the I/O address space to conveniently provide the processor with additional addresses for assignment to the various I/O devices and does not provide the similar capability to such I/O devices; namely, such I/O devices remain prohibited from access to memory above the 4 GB limit imposed by 32-bit I/O device bus and register widths.

Hence, the teachings of Jeddeloh in view of Dickey would not suggest modification of the address translation using the GART table of Jeddeloh to extend the physical address space for access to memory, as recited by ~~the claimed invention~~amended Claim 8, since the teachings of Jeddeloh are specifically limited to addressing the following problem described in the Background of Jeddeloh:

> Data transfers between processor and graphics controller, and between graphics controller and system memory are presently constrained by the bandwidth of the busses and their data channels that couple these components together. (col. 1, lines 56-60.)

As specifically indicated in the Background of Jeddeloh, what is needed is a computer system architecture that facilitates high-bandwidth data transfers between a graphics controller and other system components. (*See*, col. 2, lines 11-13.) To achieve this goal, Jeddeloh teaches data paths, which connect the graphics controller and other devices to switch 124 (FIG. 2) to have a greater width than the busses that typically couple computer system components together.

In other words, the teachings of Jeddeloh are directed to providing high-bandwidth communications and not directed to physical address range limitations caused by bus and register widths for accessing memory above the 4GB limit imposed by 32-bit bus and register widths. Furthermore, the teaching of Dickey are limited to preventing I/O fragmentation and also not directed to providing I/O device with access to memory above the 4 GB limit. Accordingly, Applicants respectfully submit that the combined teachings of Jeddeloh in view of Alpert and Dickey would not have suggested the ~~claimed invention~~above-recited features of amended Claim 8 to one of ordinary skill in the art, as required to establish a *prima facie* case of obviousness.

Therefore, for these reasons provided above amended Claim 8 is patentable over the combination of Jeddeloh in view of Dickey. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 8.

Regarding Claim 9 and 12-14, Claim 9 and 12-14 based on their dependency from Claim 8 are also patentable over the combination of Jeddeloh in view of Dickey. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the §103(a) rejection of Claim 9 and 12-14.

Regarding Claim 30, Claim 30 recites the following claim features which are neither disclosed, taught nor suggested by the combination of Jeddeloh in view of Dickey:

> a translation control circuit coupled to the address translator to program entries in the translation lookaside buffer entries to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses to enable access to the main memory above a physical address range limit imposed by a register/bus width. (Emphasis added.)

For at least the reasons indicated above, Applicants respectfully submit that the combination of Jeddeloh in view of Dickey fails to teach or suggest the programming of entries

in a translation lookaside buffer to map virtual address of a virtual memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses to enable access to the main memory above a physical address range limit imposed by a register/bus width, as in Claim 30.

Applicants respectfully submit that the features of Claim 30 are neither taught, disclosed or suggested by the combination of Jeddeloh in view of Dickey, as required to establish *prima facie* obviousness. Therefore, Applicants respectfully submit that Claim 30 is patentable over the combination of Jeddeloh in view of Dickey. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the rejection of Claim 30.

Regarding Claims 31 and 32, Claims 31 and 32, based on their dependency from Claim 30 are also patentable over the combination of Jeddeloh in view of Dickey.

The Examiner has rejected Claims 15, 17 and 19-21 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Dickey and further in view of U.S. Patent No. 5,060,137 issued to Bryg et al. ("Bryg"). Applicants respectfully traverse this rejection.

Regarding Claims 15 and 19, Claims 15 and 19 recite the following analogous claim feature ,which is neither taught nor suggested by the combination of Jeddeloh in view of Dickey and further in view of Bryg:

> control logic coupled to the translation lookaside buffer, the input register and the output register, the control logic to populate entries within the translation lookaside buffer to map virtual addresses of a memory range allocated to the graphic controller to physical addresses within main memory where the physical addresses have a greater number of bits than the virtual addresses to enable access to the main memory above a physical address range limit imposed by a register/bus width. (Emphasis added.)

For at least the reasons previously indicated above with regard to the rejection of Claims 8 and 30, the combination of Jeddeloh in view of Dickey fails to teach or suggest the expansion of a physical address range for access to main memory above a physical address limit imposed by a register/bus width by providing a mapping of virtual addresses to physical addresses where the physical addresses have a greater number of bits than the virtual addresses, as recited by Claims 15 and 19.

Regarding the Examiner's citing of Bryg, Applicants respectfully submit that the Examiner's citing of Bryg fails to rectify the deficiencies of the combination of Jeddeloh in view of Campbell to teach the control logic coupled to the translation lookaside buffer to populate entries within the translation lookaside buffer to map the virtual addresses of a virtual memory range allocated to the graphics controller to physical addresses within the main memory where the physical addresses have a greater number of bits than the virtual addresses, as recited by Claims 15 and 19.

Applicants respectfully submit that the references of record are not directed to overcoming a physical address range limit such as, for example, the 4 Gb physical address range limit imposed by conventional 32-bit registers and busses. Hence, although Dickey expands the I/O address space for the various bridges and peripheral devices connected to a computer system as taught by Dickey, this expansion is simply limited to the processor's view. In other words, Dickey teaches expansion of the I/O address space to conveniently provide the processor with additional addresses for assignment to the various I/O devices and does not provide the similar capability to such I/O devices; namely, such I/O devices remain prohibited from access to memory above the 4 GB limit imposed by 32-bit I/O device bus and register widths. ~~Although Dickey discloses the use of _____. As taught by Dickey,~~ _____.

Applicants respectfully submit that the absence within Dickey of any disclosure, teaching or suggestion regarding the expanding of a received virtual address to a physical address for access to main memory, where the physical address has a greater number of bits than the virtual address to enable access to the main memory above a physical address range limit imposed by a register/bus width, as recited by Claims 15 and 19, prevents the Examiner from establishing a *prima facie* case of obviousness of Claims 15 and 19.

Consequently, Applicants respectfully submit that Claims 15 and 19 are patentable over the combination of Jeddeloh in view of Dickey and further in view of Bryg. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the §103 rejection of Claims 15 and 19.

Regarding Claims 17, 20 and 21, Claims 17, 20 and 21, based on their dependency from Claims 15 and 19, respectively, are also patentable over the combination of Jeddeloh in view of Campbell and further in view of Bryg. Therefore, Applicants respectfully request the Examiner reconsider and withdraw the § 103 rejection of Claims 17, 20 and 21.

CONCLUSION

In view of the foregoing, it is submitted that Claims 8, 9, 12-15, 17, 19-21 and 30-32 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 3/27/07
Kumiko Alexander Date